CLAIMS

1. An electronic circuit comprising differential signal input means, a combining stage, a discriminating stage and differential signal output means, wherein the discriminating stage comprises four transistors each having respective first and second electrodes and a respective gate electrode for controlling a current flow between said first and second electrodes, wherein the first electrodes of said four transistors are connected to a common node, wherein the differential signal output means comprise a pair of differential output terminals each connected to at least one of the second electrodes of said four transistors, and wherein the combining stage is arranged to convert differential input signals received by the differential signal input means into gate signals respectively applied to the gate electrodes of at least some of said four transistors.

2. An electronic circuit as claimed in claim 1, wherein at least a first pair of gate electrodes receives a gate signal which has a common mode driven by a first differential input signal and a differential mode driven by a second differential input signal.

3. An electronic circuit as claimed in claim 1 or 2, wherein the gate signals applied to the respective gate electrodes of the four transistors of the discriminating stage are tri-state voltage signals so designed that a single one of said gate electrodes, selected from the differential input signals received by the differential signal input means, has a maximum or minimum voltage value.

4. An electronic circuit as claimed in claim 2 or 3 wherein a second pair of gate electrodes receives a gate signal which has a common mode driven by the second differential input signal and a differential mode driven by the first differential input signal.

5. An electronic circuit as claimed in claims 1, 2, 3 or 4 for providing a logic gate function, wherein the differential signal input means include two pairs of differential input terminals for respectively receiving first and second pairs of differential input data signals

wherein the combining stage includes first and second groups of four combining transistors, first current generator means for generating a first current between a first node and a first power supply terminal, second current generator means for generating a second current between a second node and the first power supply terminal, and first, second, third and fourth resistors each having a respective first end connected to the first power supply terminal and a respective second end,

wherein each of the combining transistors has respective first and second electrodes and a respective gate electrode for controlling a current flow between said first and second electrodes,

wherein the first electrodes of the four combining transistors of the first group are connected in common to said first node, and the first electrodes of the four combining transistors of the second group are connected in common to said second node,

wherein the first pair of differential input data signals includes a signal (b) applied to the gate electrodes of two combining transistors (Q0, Q1) of the first group, which combining transistors have their second electrodes connected to the second ends of said first and second resistors respectively, and a signal (bq) applied to the gate electrodes of the two other combining transistors (Q2, Q3) of the first group, which other combining transistors have their second electrodes connected to the second ends of said third and fourth resistors respectively,

wherein the second pair of differential input data signals includes a signal (a) applied to the gate electrodes of two combining transistors (Q4, Q6) of the second group, which combining transistors of the second group have their second electrodes connected to the second ends of said first and third resistors respectively, and a signal (aq) applied to the gate electrodes of the two other combining transistors (Q5, Q7) of the second group, which other combining transistors of the second group have their second electrodes connected to the second ends of said second and fourth resistors respectively,

and wherein the second ends of the first, second, third and fourth resistors are connected to the gate electrodes of the four transistors of the discriminating stage respectively.

6. An electronic circuit as claimed in claim 5 for providing a logic AND or NOR function, wherein said pair of differential output terminals has a first terminal connected to the second electrodes of three of the four transistors of the discriminating stage, which transistors have their respective gate electrodes connected to the second ends of said first, second and third resistors, and a second terminal connected to the second electrode of the other one of the four transistors of the discriminating stage, which other transistor has its grating electrode connected to the second end of said fourth resistor.

7. An electronic circuit as claimed in claim 5 for providing a logic OR or NAND function, wherein said pair of differential output terminals has a first terminal connected to the second electrode of one of the four transistors of the discriminating stage, which transistor has its gate electrode connected to the second end of said first resistor, and a second terminal connected to the second electrodes of the three other ones of the four transistors of the discriminating stage, which three transistors have their respective grating electrodes connected to the second ends of said second, third and fourth resistors.

8. An electronic circuit as claimed in claim 5 for providing a logic EXCLUSIVE OR function, wherein said pair of differential output terminals has a first terminal connected to the second electrodes of two of the four transistors of the discriminating stage, which two transistors have their respective gate electrodes connected to the second ends of said second and third resistors, and a second terminal connected to the second electrodes of the other two of the four transistors of the discriminating stage, which other two transistors have their respective grating electrodes connected to the second ends of said first and fourth resistors.

9. An electronic circuit as claimed in claim 1 or 2 for providing a latch function, wherein the differential signal input means include a pair of differential input

terminals for receiving differential latch control signals, wherein the differential output terminals are respectively connected to the gate electrodes of two of said four transistors for applying thereto respective gate signals corresponding to differential output signals of the circuit, and wherein the combining and discriminating stages are so arranged that the gate signals provided by the combining stage have voltage levels higher than said differential output signals in a first state of the differential latch control signals and lower than said differential output signals in a second state of the differential latch control signals.

10. An electronic circuit as claimed in claim 9, wherein the differential signal input means further include a pair of differential input terminals for receiving a pair of differential input data signals,

wherein the combining stage includes a first group of four combining transistors, a second group of two combining transistors, first current generator means for generating a first current between a first node and a first power supply terminal, second current generator means for generating a second current between a second node and the first power supply terminal, and first and second resistors each having a respective first end connected to first power supply terminal and a respective second end,

wherein the discriminating stage further includes third and fourth resistors having respective first ends connected to a second power supply terminal and second ends respectively connected to the pair of differential output terminals,

wherein each of the combining transistors has respective first and second electrodes and a respective gate electrode for controlling a current flow between said first and second electrodes,

wherein the first electrodes of the four combining transistors of the first group are connected in common to said first node, and the first electrodes of the two combining transistors of the second group are connected in common to said second node,

wherein the pair of differential latch control signals includes a signal (clk) applied to the gate electrodes of two combining transistors (Q0, Q1) of the first group, which combining transistors have their second electrodes connected to the second ends of said first and second resistors respectively, and a signal (clkq) applied to the gate

electrodes of the two other combining transistors (Q2, Q3) of the first group, which other combining transistors have their second electrodes connected to the second ends of said third and fourth resistors respectively,

wherein the pair of differential input data signals includes a signal (a) applied to the gate electrode of one combining transistor (Q4) of the second group, which combining transistor has its second electrode connected to the second end of said first resistor, and a signal (aq) applied to the gate electrode of the other combining transistor (Q5) of the second group, which other combining transistor has its second electrode connected to the second end of said second resistor,

and wherein said four transistors of the discriminating stage include a transistor (Q8) having its gate electrode connected to the second end of the second resistor and its second electrode connected to the second end of the third resistor, a transistor (Q9) having its gate electrode connected to the second end of the fourth resistor and its second electrode connected to the second end of the third resistor, a transistor (Q10) having its gate electrode connected to the second end of the third resistor and its second electrode connected to the second end of the fourth resistor, and a transistor (Q11) having its gate electrode connected to the second end of the first resistor and its second electrode connected to the second end of the fourth resistor.

11. An electronic circuit according to claim 1 wherein combining stage comprises:

- a first pre-combining stage, a first pre-discriminating stage and first differential signal intermediate means, wherein the first pre-discriminating stage comprises four transistors each having respective first and second electrodes and a respective gate electrode for controlling a current flow between said first and second electrodes, wherein the first electrodes of said four transistors are connected to a common node, wherein the first differential signal intermediate means comprise two pairs of first differential intermediate terminals each connected to two of the second electrodes of said four transistors, and wherein the first pre-combining stage is arranged to convert a first pair of differential input signals received by the differential signal input means into gate signals applied to the gate electrodes of at least some of said four transistors of first pre-discriminating stage respectively,

- a second pre-combining stage, a second pre-discriminating stage and second differential signal intermediate means, wherein the second pre-discriminating stage comprises four transistors each having respective first and second electrodes and a respective gate electrode for controlling a current flow between said first and second electrodes, wherein the first electrodes of said four transistors are connected to a common node, wherein the second differential signal intermediate means comprise two pairs of second differential intermediate terminals each connected to at least two of the second electrodes of said four transistors, and wherein the second pre-combining stage is arranged to convert a second pair of differential input signals received by the differential signal input means into gate signals applied to the gate electrodes of at least some of said four transistors of second discriminating stage respectively,

and wherein the combining stage is arranged to convert intermediate signals received by first and second differential intermediate terminals into the gate signals applied to the grating electrodes of at least some of said four transistors of discriminating stage respectively.